Field

The present invention relates to electronic systems, and more particularly, to a bus.

Background

A GTL (Gunning Transceiver Logic) bus is well-known, where an example of an electronic system utilizing a GTL bus having nMOSFET (n-Metal Oxide Semiconductor Field Effect Transistor) driver **102** is illustrated in Fig. 1. In the example of Fig. 1, two agents are connected to transmission line **104** to receive signals from nMOSFET driver **102**. An agent may be a microprocessor, memory device, or any other electronic device for sending or receiving signals along transmission line **104**. Resistors R_T are termination resistors to reduce reflections at the ends of transmission line **104**, and are connected to a voltage source providing a termination voltage V_{TT}. Resistor R_{ESD} is a resistor to reduce the probability of electrostatic discharge damage to nMOSFET driver **102**, and may not be needed for some applications. The gate of nMOSFET driver **102** is driven according to a digital data signal so as to switch nMOSFET driver **102** ON and OFF to drive transmission line **104**.

The ideal (quiescent or steady state) voltage of transmission line **104** is in the range $[V_{TT} - V_{SW}, V_{TT}]$, where the voltage swing V_{SW} is given by $V_{SW} = V_{TT}[(R_T/2)/(R_{ONn} + R_{ESD} + R_T/2)]$ and where R_{ONn} is the ON resistance of nMOSFET driver **102**. Because of impedance mismatch due to mismatches between nMOSFET driver **102**, termination resistor R_T, and transmission line **104**, as well as stubs **106** and other artifacts, the actual signal voltage propagating along transmission line **104** will have over-shoots and under-shoots outside the ideal or quiescent voltage range. Note that in the above lumped-parameter equation for V_{SW}, the resistance R_{ESD} adds to the resistance R_{ONn}. When R_{ESD} is present, nMOSFET driver **102** needs to be designed with smaller R_{ONn} than when R_{ESD} is not present in order to maintain the same voltage swing on transmission line **104**. However, reducing R_{ONn} increases the size of nMOSFET driver **102**, which increases the impedance mismatch.

In addition to distributing the core voltage V_{CC} in an electronic system, GTL busses also require distributing the termination voltage V_{TT}, which may result in added system cost due to extra motherboard power planes, wiring, pins, etc. Furthermore, with

new process technologies allowing for smaller core voltages than in the past, signal over-shoots above V_{TT} may be too large for the oxide thickness of new process technologies. This problem may be alleviated by lowering the termination voltage, but then the voltage range $[V_{TT} - V_{SW}, V_{TT}]$ of transmission line **104** will be shifted, which may require a re-design of agents connected to the transmission line. Embodiments of the present invention address some or all of these problems.

Summary

Embodiments of the present invention are directed to a bus in which a terminated transmission line is excited by a pMOSFET, where the transmission line is terminated by connecting at least one termination device between the transmission line and ground. In one embodiment, the pMOSFET has its drain connected to the transmission line and its source biased to a core voltage V_{CC}.

Brief Description of the Drawings

Fig. 1 illustrates a prior art GTL bus.

Fig. 2 illustrates an exemplary bus according to the present invention.

Fig. 3 illustrates another exemplary bus according to the present invention.

Detailed Description of Embodiments

An embodiment of the present invention is illustrated in Fig. 2. In Fig. 2, pMOSFET driver (pullup) **202** drives transmission line **204** according to a data signal applied to its gate. The source of pMOSFET driver **202** is at a voltage V_{CC}. V_{CC} may, but need not be, a processor core voltage. Resistors R_T provide termination to transmission line **204** so as to reduce reflections and provide a pulldown to substrate voltage V_{SS}. The substrate voltage V_{SS} may also be termed a ground voltage, and the terms ground and substrate may be used interchangeably.

In practice, pMOSFET driver **202** may actually comprise a plurality of pMOSFETs coupled in parallel, where some subset of the plurality of pMOSFETs have their gates enabled to be responsive to the data signal. In this way, the effective ON resistance of pMOSFET driver **202** may be adjusted by proper choice of the enabled subset. It is therefore to be understood in this specification and the following claims that a pMOSFET driver may also include a plurality of parallel coupled pMOSFETs in which all or some proper subset of the plurality are enabled.

By terminating transmission line **204** to V_{SS}, a separate voltage source for V_{TT} is not needed as in some prior art busses. Furthermore, the ideal voltage range of transmission line **204** is $[V_{SS}, V_{SS} + V_{SW}]$, where the swing voltage V_{SW} is given by $V_{SW} = V_{CC}[(R_T/2/(R_{ONp} + R_T/2)]$ and where R_{ONp} is the ON resistance of pMOSFET driver **202**. The ideal voltage range is referenced to V_{SS}, and thus embodiments of the present invention may be better suited to bridging different process technologies than prior art busses.

For many practical situations, the embodiment of Fig. 2 exhibits some other advantages over the embodiment of Fig. 1. For example, when the voltage swings of the embodiments of Figs. 1 and 2 are equal, it is found that the driver of the present embodiment may be better matched to the transmission line characteristic impedance. As a specific example, consider the case in which a 60Ω transmission line is terminated at both ends with 60Ω resistors, and where the voltage swing is 1.0V. For an embodiment of the present invention according to Fig. 2, the output impedance of pMOSFET **202** is 15Ω if $V_{CC} = 1.5$V. However, for the example of prior art Fig. 1, the sum of the output impedance of nMOSFET **102** with resistor R_{ESD} is 15Ω if $V_{TT} = 1.5$V. Since $R_{ESD} > 0$, the output impedance of nMOSFET **102** is less than 15Ω, and thus there is greater mismatch than in the embodiment of Fig. 2.

Another advantage of some of the embodiments is that to maintain the same voltage swing, pMOSFET **202** may be similar or smaller in size than nMOSFET **102** without sacrificing driver strength. Also, because pMOSFETs are less susceptible to electrostatic discharge damage, for many applications an electrostatic discharge resistor is not needed for pMOSFET driver **202**. This allows greater flexibility in its manufacturing process. Furthermore, the use of pMOSFETs with an n-well process may be advantageous in that substrate noise may be reduced, which may be particularly advantageous for so-called systems-on-chip designs.

The embodiment of Fig. 2 may be modified in various ways. For example, termination resistors R_T may be replaced with on-chip nMOSFETs. Note that adding electrostatic discharge resistors R_{ESD} to such nMOSFETs not only provide the function of reducing the probability of electrostatic discharge, but they also linearize the effective

resistance termination of the nMOSFETs in combination with the resistors R_{ESD} so as to provide better termination of the transmission line.

Another embodiment of the present invention is provided in Fig. 3, which is applicable to high speed, point-to-point busses in which it is particularly advantageous for a driver's impedance to be matched to a transmission line. However, it is not necessary for the driver's impedance to be matched to the transmission line. In Fig. 3, in addition to pMOSFET driver **202** and transmission line **204**, is nMOSFET driver **302** and combinational logic circuit **304**. nMOSFET driver **302** is shown as comprising a plurality of nMOSFETs **305** having gates connected to output ports **306** of combinational logic circuit **304**. The input port **308** of combinational logic circuit **304** is responsive to the same digital data signal that drives the gate of pMOSFET driver **202**. It is to be understood in this specification and the following claims that a nMOSFET driver may also include a plurality of parallel coupled nMOSFETs in which all or some proper subset of the plurality are enabled.

The input-output relationship of combinational logic circuit **304** is such that when input port **308** is LOW, a subset of nMOFETs **305** is switched ON so that the parallel combination of the ON resistance of nMOSFET driver **302** with the ON resistance of pMOSFET driver **202** is substantially matched to the characteristic impedance of transmission line **204**; whereas when input port **308** is HIGH, the effective ON resistance of nMOSFET driver **302** is substantially matched to the characteristic impedance of transmission line **204**. In this way, the impedance of the combination of pMOSFET driver **202** and nMOSFET driver **302** is matched to transmission line **204**.

The embodiment of Fig. 3 may also be used in a differential signaling scheme, where in addition to the circuit of Fig. 3 another circuit identical to that of Fig. 3 is also employed but in which it is driven by a data signal complementary to the data signal that drives the circuit of Fig. 3.

Various modifications may be made to the disclosed embodiments without departing from the scope of the invention as claimed below.